# Application/Control No. 09/754,406 Examiner Mary C Hogan Applicant(s)/Patent Under Reexamination XU, SONGJIE Art Unit Page 1 of 1

# Notice of References Cited

### U.S. PATENT DOCUMENTS ,

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	Α	US-		( 75)	
	B√	TUS-		1,	
	C.	US-		2	
	D	US-			
	E	US-			
	F	US-			
	G	US-			, ,
	Н	US-			
	1	US-			
	J	US-			
	К	US-			
	L	US-			
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### **FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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	Q					
	R	-				
	S					
	Т					

## **NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Singh, K.J., "Performance Optimization of Digital Circuits, Ph.D. Dissertation, University of California Berkley, 1992
	٧	Singh et al, "Timing Optimization of Combinational Logic", Computer-Aided Design, 1988. ICCAD-88. Digest of Technical Papers., IEEE International Conference, 7-10 Nov. 1988, Pages:282 – 285
	w	
	х	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

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